R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a data controller for use within a peripheral device having a storage medium. The data controller generally comprises a transfer extend generator and at least one retrieval channel. The transfer extend generator may be configured to generate transfer extend entries for a data transfer between the storage medium and a host computer. Each of the transfer extend entries may comprise a pointer to a next transfer extend entry. The at least one retrieval channel may be configured to receive the transfer extend entries for programming the data transfer.

SUPPORT FOR SPECIFICATION AND CLAIM AMENDMENTS

Support for the amendment to the claims may be found, for example, in FIG. 3 as originally filed and, for example, on page 3/ lines 26-29 and page 11/lines 1-24 of the specification, as originally filed. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejections of claims 2, 3 and 12 under 35 U.S.C. §102(e) as being anticipated by Ellis et al., U.S. Patent No.

6,029,226, has been obviated by appropriate amendment and should be withdrawn.

Ellis et al. disclose a method and apparatus for writing data to a storage device such as a hard disk in which two write commands from an initiator are processed as a single command at the storage device. During a write operation, an ending logical block address (LBA) of a first write command may be compared to a starting LBA of a second (subsequent) write command. If the starting LBA is within a selected range of the ending LBA, then the second write command is "coalesced" or merged with the first write command. The merged first and second write commands are then presented to the storage medium as a single disk command.

In contrast, the independent claim 2 includes re-ordering the commands received from the host computer. The re-ordering may change the sequence of commands from an order of arrival to an order of sequence in the storage medium. Ellis et al. only disclose handling write commands in the order of arrival. Since the Ellis et al. do not disclose or suggest that the second write command can be re-ordered before the first write command, then claim 2 is fully patentable over Ellis et al. and the rejection should be withdrawn.

Claim 3 includes a command queuing engine that creates a plurality of threads of sequential commands simultaneously. Ellis et al. disclose creating one thread at any given time from two

write commands. However, Ellis et al. do not disclose or suggest creating multiple threads simultaneously as presently claimed. Therefore, claim 3 is fully patentable over Ellis et al. and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1 and 5-11 under 35 U.S.C. §103(a) as being unpatentable over Garrett et al. '842 in view of Bean et al. '626, has been obviated by appropriate amendment and should be withdrawn. The rejection of claims 13-20 under 35 U.S.C. §103(a) as being unpatentable over Ellis et al. in view of Bean et al. has been obviated by appropriate amendment (to the independent claims) and should be withdrawn. The rejection of claim 4 under 35 U.S.C. §103(a) as being unpatentable over Ellis et al. in view of Krakirian, U.S. Patent No. 5,781,803 has been obviated by appropriate amendment (claim 4 has been cancelled) and should be withdrawn.

Garrett et al. disclose a method for transferring data between non-contiguous buffers in a memory 12 of a host computer and a FIFO 25 of an I/O device 10 via a system bus 14. The method uses a descriptor queue stored in the memory 12. Each descriptor points to a buffer and includes the length of the buffer. When data is to be transferred, a device driver software located in a processor 11 of the host computer sends the number of available

descriptors to the I/O device 10. The I/O device 10 then accesses the descriptors individually or in a burst mode to gain access to data within the buffers identified by the descriptors.

Bean et al. disclose an apparatus and a method for controlling digital data processing in a system employing multiple processors. Each command received by the system is associated with a control block 49 and a route 36. Each route 36 comprises a sequence of route vectors 38. Each route vector 38 identifies an operation to be performed to execute the command as well as the process, or station, to execute the route vector 38. The control block 49 is first sent to a work queue 58 of the station to perform the first operation. When the station gets the control block 49, the station performs the operation required by the route vector 38, modifies the control block 49 to identify the next route vector 38 in the sequence, and transfers the control block 49 to the work queue 58 of the station to perform the operation required by the next route vector 38 in the route 36. A head pointer 60 of the work queue 58 points to the first control block 49 in the work queue 58. A tail pointer 61 of the work queue 58 points to the last control block 49 in the work queue 58.

In contrast, claim 1 provides that each transfer extend entry has a pointer to a next transfer extend entry. While Garrett et al. disclose a pointer within the descriptors, the pointers of Garrett et al. point to data buffers within a memory 12 of the host

computer. While Bean et al. disclose route vectors within the control blocks, the route vectors point to the stations assigned to perform the work defined in the control block. Even if (despite the lack of motivation) Garrett et al. is combined with Bean et al., the combination does not teach or suggest a pointer within each transfer extend entry that points to the next transfer extend entry. Consequently, claim 1 is fully patentable over the cited rejections and should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 810-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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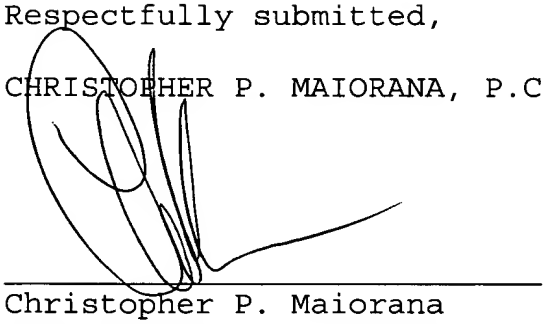

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (THREE TIMES AMENDED) A data controller of a peripheral device having a storage medium, the data controller comprising:

a transfer extend generator that generates transfer extend entries for a data transfer between the storage medium and a host computer, each of said transfer extend entries comprising a pointer to a next transfer extend entry; and

at least one retrieval channel coupled to receive the transfer extend entries for programming the data transfer.

2. (TWICE AMENDED) A data controller of a peripheral device having a storage medium and a processor, wherein the data controller minimizes interrupts to the processor by [processing] re-ordering a plurality of [sequential] commands received from a host computer from an order of arrival into an order of sequence in the storage medium.

3. (TWICE AMENDED) A data controller, that is couplable to a host and coupled to a storage medium, microprocessor, local storage and a buffer memory, comprising a command queuing engine that creates [and executes] a plurality of threads of sequential commands simultaneously while minimizing interrupts associated to the commands.

12. (TWICE AMENDED) The data controller of claim 2, further comprising a command queueing engine configured to arrange the plurality of [sequential] commands into at least one thread.